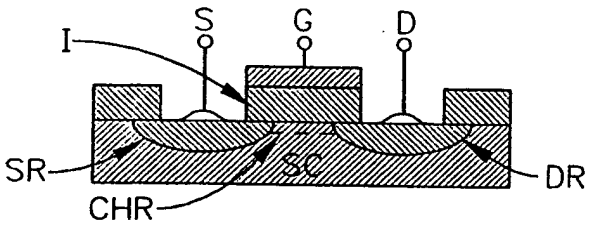

FIG. 1

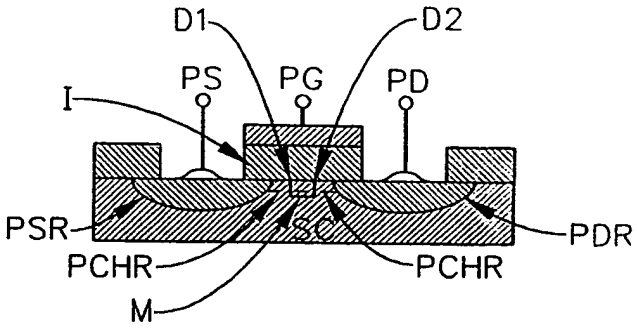

FIG. 2

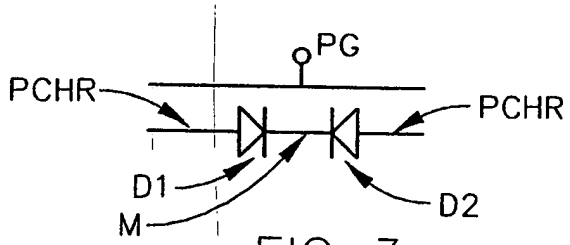

FIG. 3

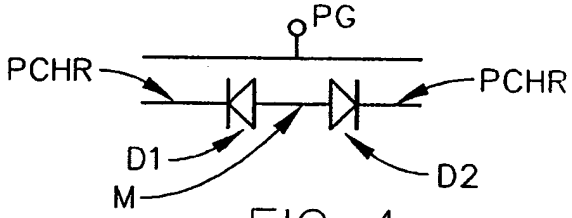

FIG. 4

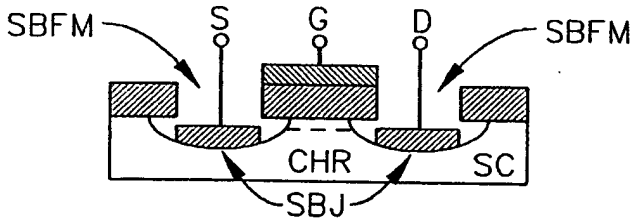

FIG. 5

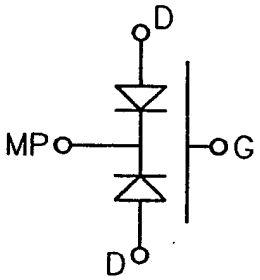

FIG. 6a

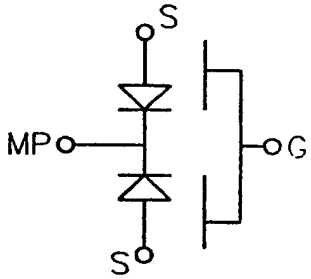

FIG. 7a

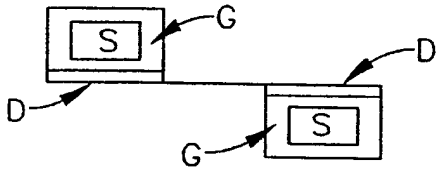

FIG. 9a

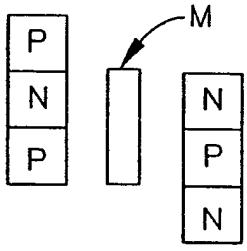

FIG. 9b

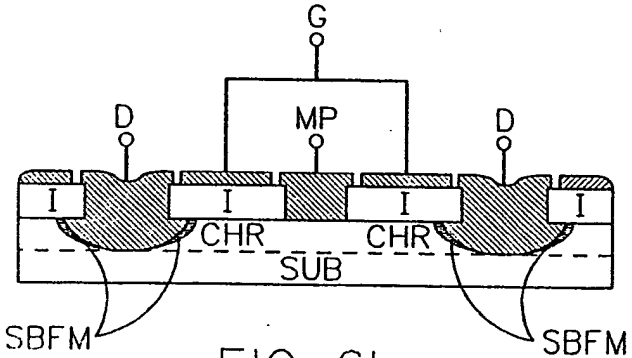

FIG. 6b

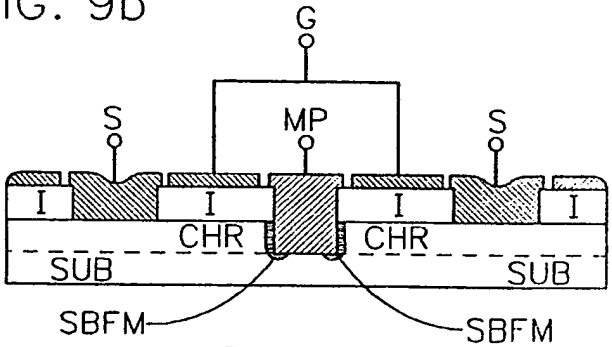

FIG. 7b

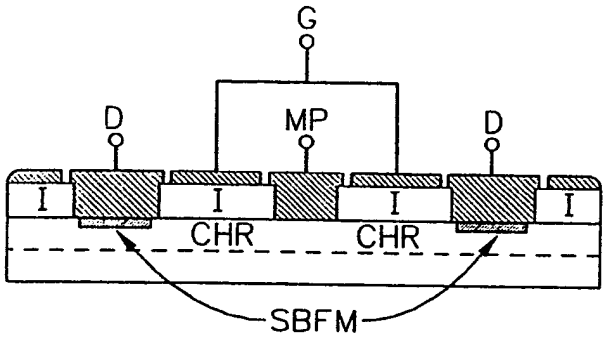

FIG. 6c

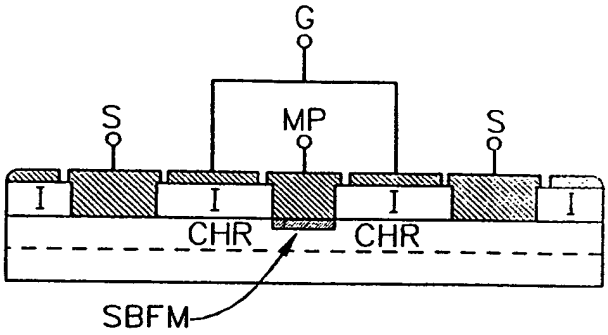

FIG. 7c

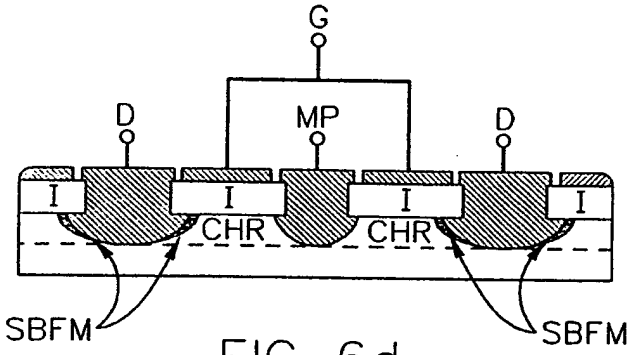

FIG. 6d

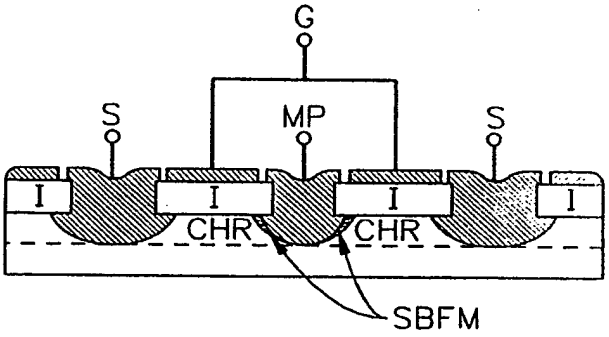

FIG. 7d

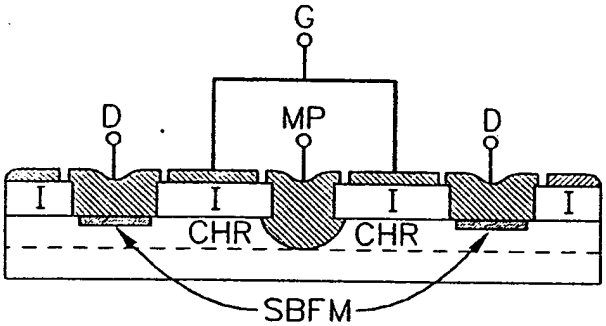

FIG. 6e

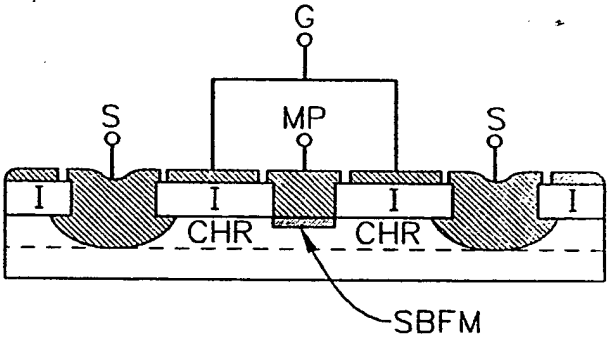

FIG. 7e

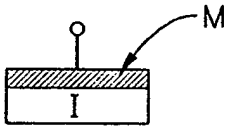

FIG. 6f

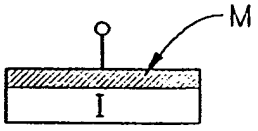

FIG. 7f

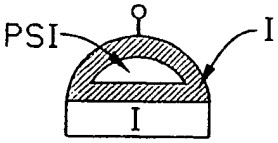

FIG. 6g

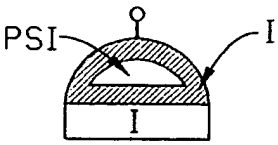

FIG. 7g

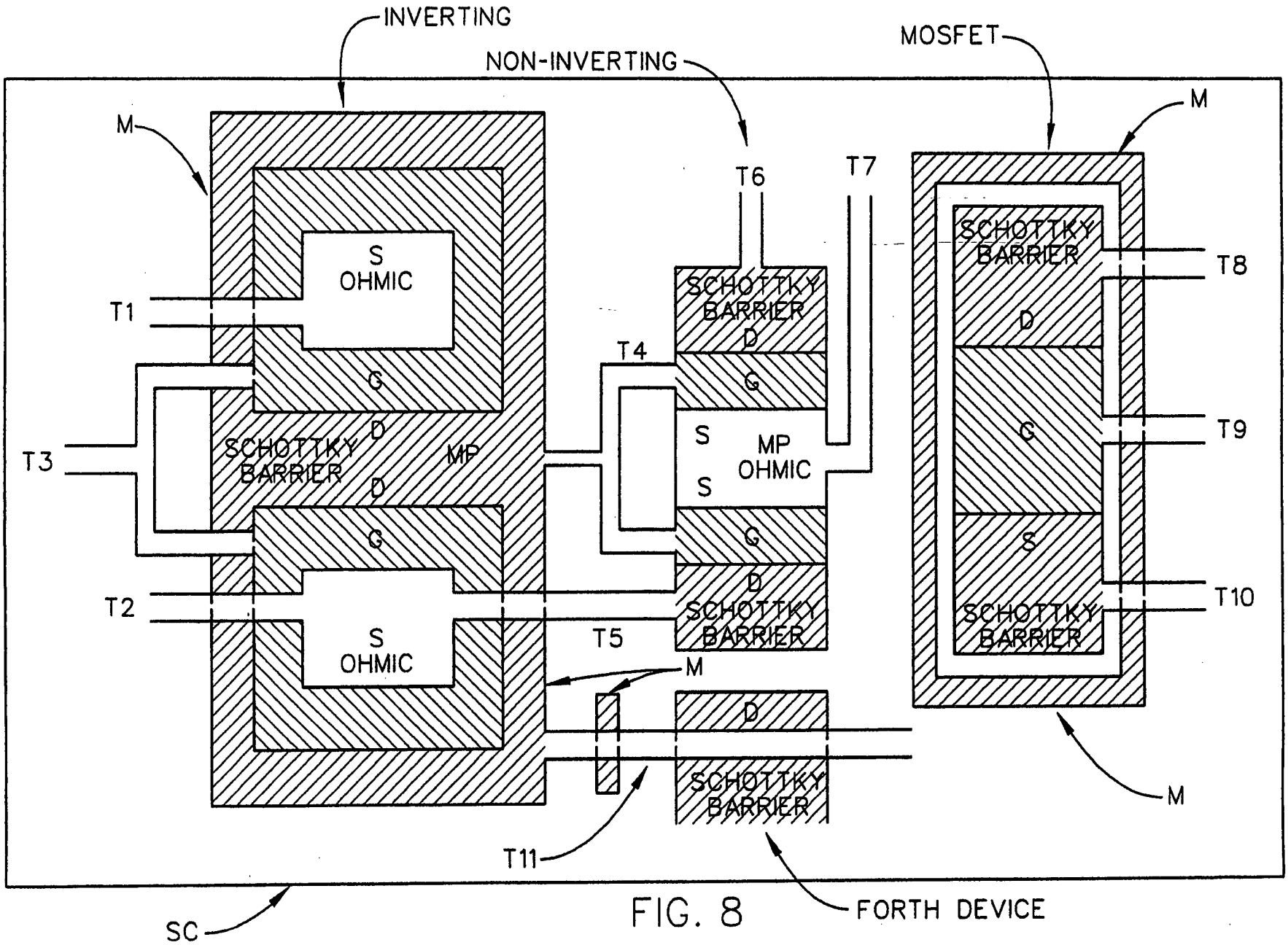
INVERTING
NON-INVERTING
MOSFET
M
M
M
M
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
S
OHMIC
G
D
SCHOTTKY
BARRIER
MP
S
MP
OHMIC
S
OHMIC
SCHOTTKY
BARRIER
SC
FORTH DEVICE

FIG. 8

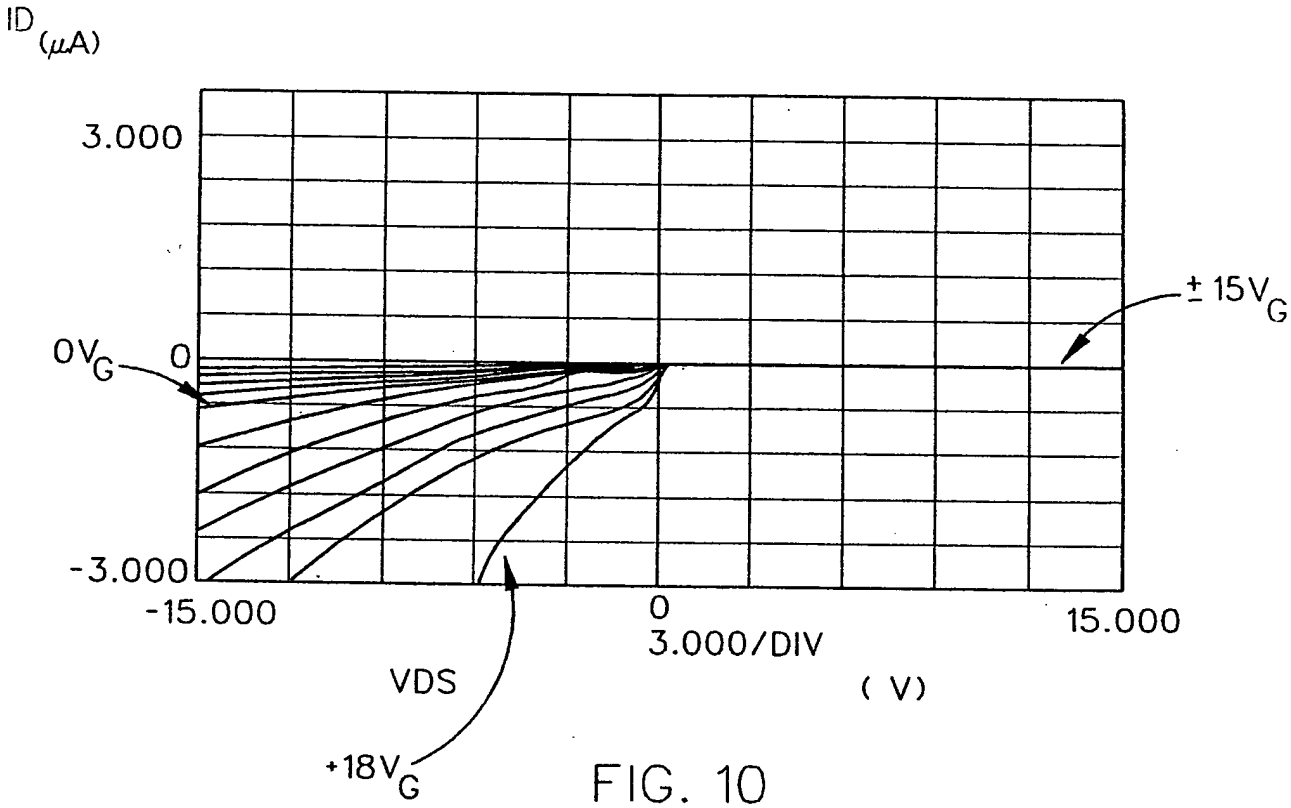
ID (μA)
3.000
0
-3.000
0VG
±15VG
-15.000
0
15.000
3.000/DIV
(V)
VDS
+18VG

FIG. 10

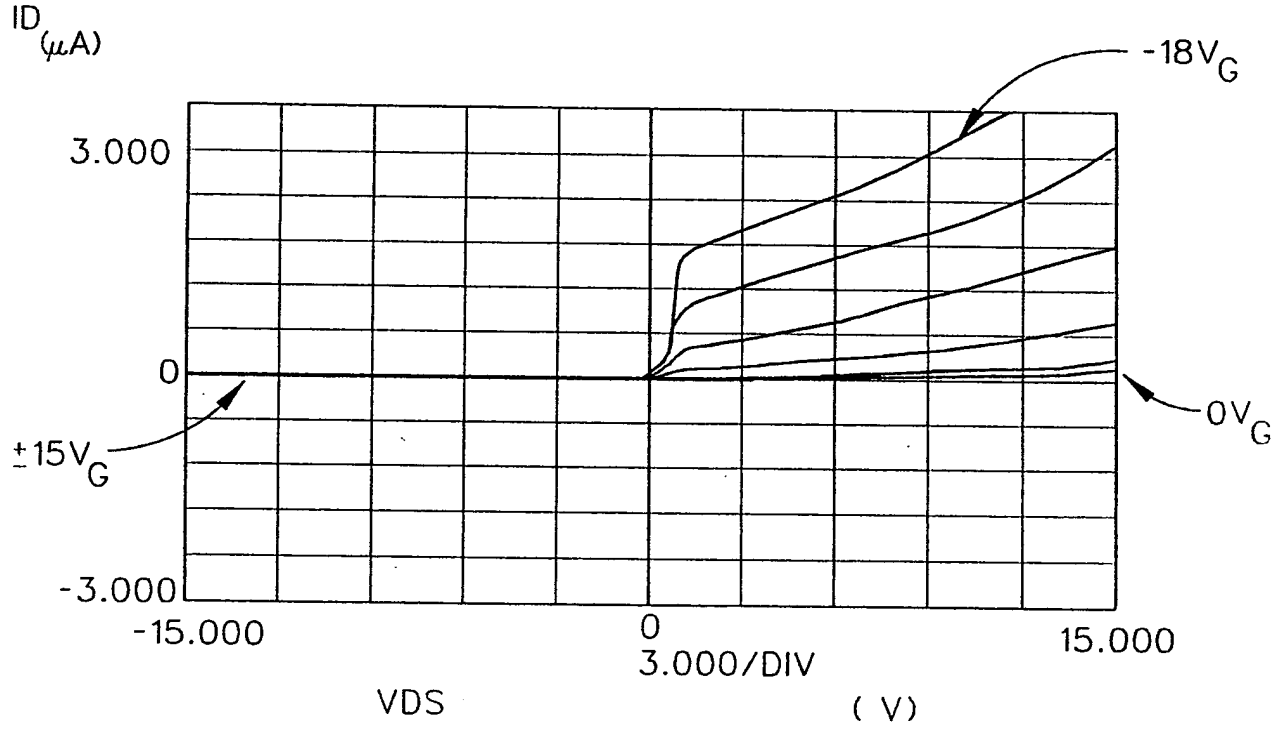
ID (μA)
3.000
0
-3.000
-18VG
±15VG
0VG
-15.000
0
15.000
3.000/DIV
(V)
VDS

FIG. 11

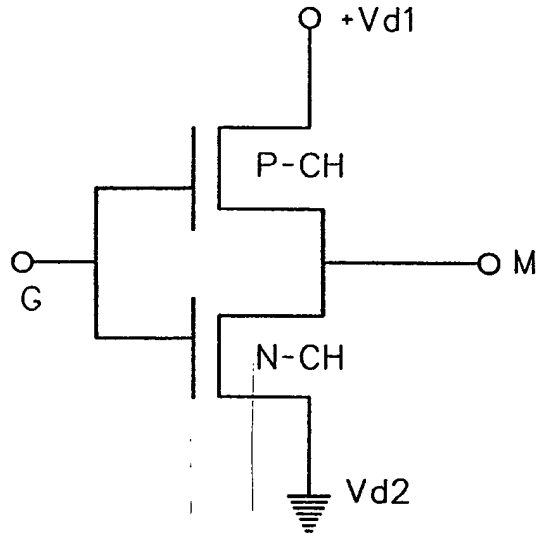

FIG. 12a

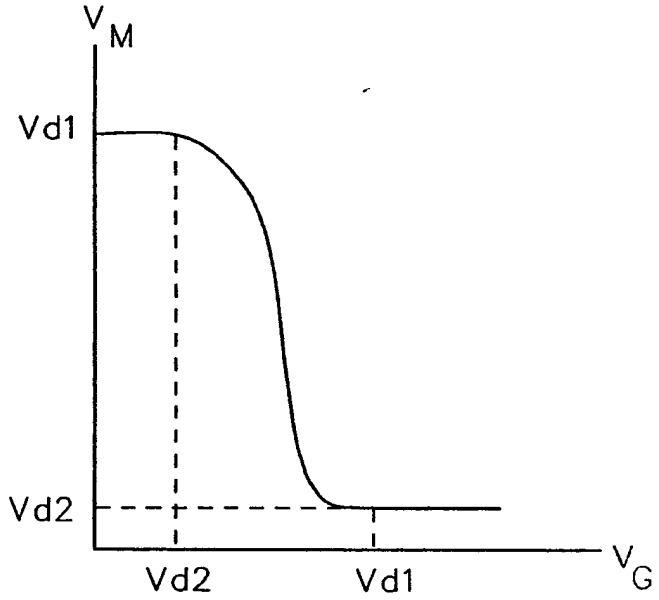

FIG. 12b

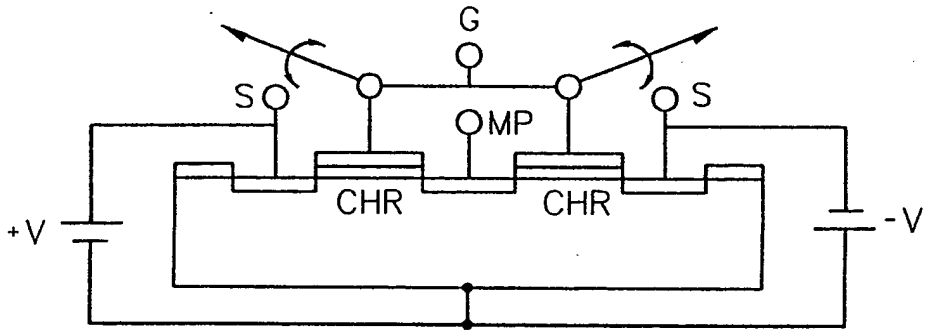

FIG. 13a

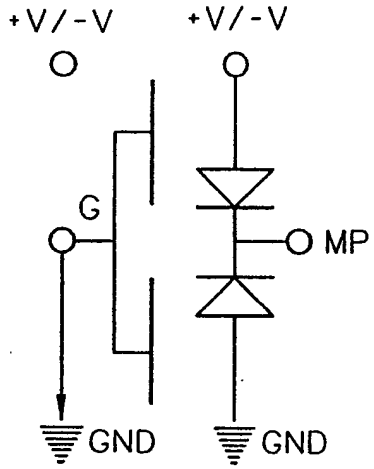

FIG. 13b

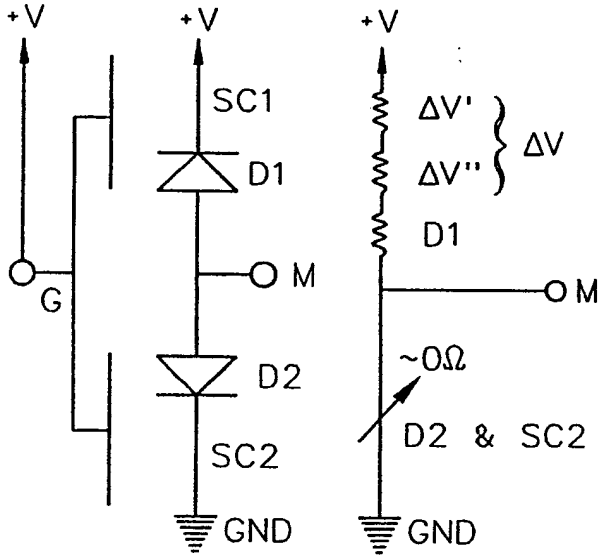

FIG. 14a

ΔV' = PINCHOFF VOLTAGE DROP

ΔV'' = SILICON CHANNEL VOLTAGE DROP

ΔV = ΔV' + ΔV'' & IS "OFF" HALF SILICON CHANNEL CARRIER INDUCING GATE VOLTAGE

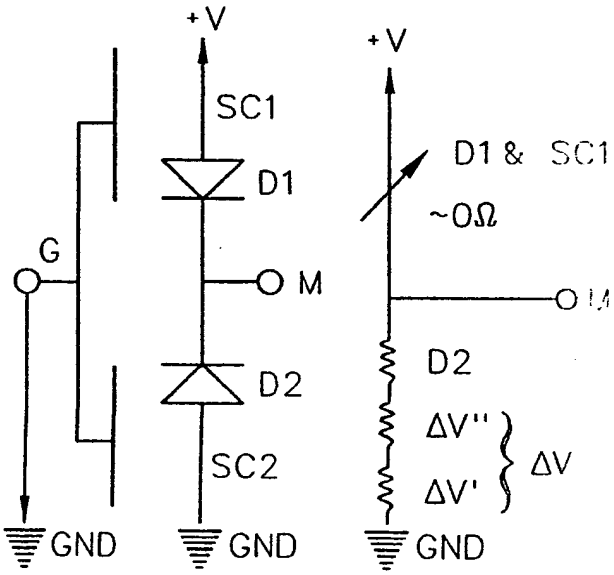

FIG. 14b

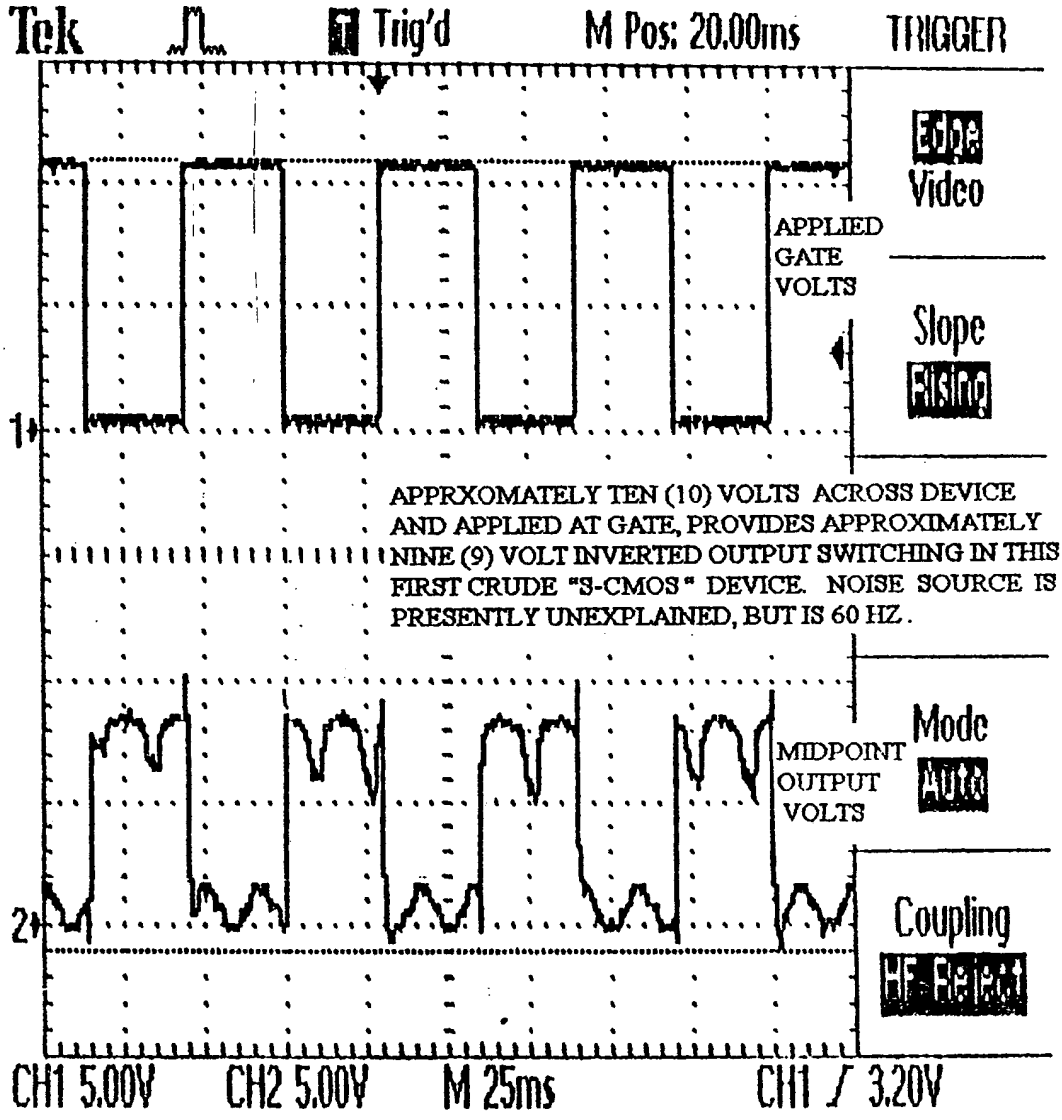
Tek
Trig'd
M Pos: 20.00ms
TRIGGER
Edge
Video
APPLIED
GATE
VOLTS
Slope
Rising
APPRXOMATELY TEN (10) VOLTS ACROSS DEVICE
AND APPLIED AT GATE, PROVIDES APPROXIMATELY
NINE (9) VOLT INVERTED OUTPUT SWITCHING IN THIS
FIRST CRUDE "S-CMOS" DEVICE. NOISE SOURCE IS
PRESENTLY UNEXPLAINED, BUT IS 60 HZ.
Mode
Auto
MIDPOINT
OUTPUT
VOLTS
Coupling
CH1 5.00V
CH2 5.00V
M 25ms
CH1 3.20V

FIG. 15